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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, HETUL B	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,795	KILBUCK ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-99* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-99* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/04/2007 has been entered.

2. Applicant's arguments filed on May 04, 2007 have been considered but they are not persuasive.

3. The rejection of claims 1-99 as in the final office action mailed on 02/05/2007 is respectfully maintained and reiterated below for Applicant's convenience.

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The clear support and antecedent basis is not found for the term "an external synchronous memory interface" in the specification of the current application in such a way so that the meaning of the terms in the claims may be ascertainable by reference to the description.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-99 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-99 are rejected under 35 U.S.C. 112, second paragraph because a person of skill in the art would not be able to ascertain the metes and bound of the claimed invention, specifically, for the term "an external synchronous memory interface" used in claims 1-99. For purpose of examination, the term "an external synchronous memory interface" is interpreted as synchronous memory interface. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 10-13, 17-22, 27-28, 34-35, 39-46, 52, 54-61, 67-68, 70-75, 79-80, 86-87 and 89-99 are rejected under 35 U.S.C. 102(e) as being anticipated by Zitlaw et al. (USPN: 2004/0128425) hereinafter, Zitlaw

The applied reference has a common assignee and inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 1, Zitlaw teaches a non-volatile memory device (i.e. 150 in Fig. 1B) comprising:

- a non-volatile memory array (i.e. 158 and 160 in Fig. 1B);
- a buffer memory (i.e. 156 in Fig. 1B);
- a synchronous memory interface (i.e. 154 in Fig. 1B); and
- a controller (i.e. 152 in Fig. 1B) coupled to the non-volatile memory array, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and buffer memory and to present the non-volatile memory device as a synchronous memory device through the synchronous memory interface (e.g. see Fig. 1B and paragraph [0036]).

As per claim 10, Zitlaw teaches the claimed invention as described above and furthermore, Zitlaw teaches that the non-volatile memory array (i.e. 158 and 160 in Fig. 1B) of the non-volatile memory device (i.e. 150 in Fig. 1B) is a synchronous flash memory array (i.e. each SDRAM memory can be replaced with the SyncFlash memory as described in the paragraph [0006]), i.e. one of a NAND architecture Flash memory array, a NOR architecture Flash memory array, EEPROM memory array, Polymer Memory array, Ferroelectric Random Access Memory array (FeRAM), Ovionics Unified Memory array (OUM), Magnetoresistive Random Access Memory array (MRAM), Molecular Memory array, and Carbon Nanotube Memory array (e.g. see paragraph [0037] and Fig. 1B).

As per claim 11, Zitlaw teaches the claimed invention as described above and furthermore, Zitlaw teaches that the synchronous interface is a SDRAM interface memory bus (i.e. 154 in Fig. 1B), i.e. one of a SDRAM interface, a DDR interface, a DDR2 interface, GDDR interface, GDDR2 interface, and RDRAM interface (e.g. see paragraph [0036] and Fig. 1B).

As per claim 12, Zitlaw teaches the claimed invention as described above and furthermore, Zitlaw teaches that the non-volatile memory device is adapted to present through the synchronous interface as SDRAM or DDR-SDRAM (160 in Fig. 1B), i.e. one of a compatible read/write capable SDRAM device, a DDR device, a DDR2 device, a GDDR device, a GDDR2 device, and a RDRAM device (e.g. see paragraph [0036]).

As per claim 13, Zitlaw teaches the claimed invention as described above and furthermore, Zitlaw teaches that the non-volatile memory device is adapted to act as a

BIOS boot memory device (i.e. the synchronous flash boot memory, 168 in Fig. 1B) (e.g. see paragraph [0037] and Fig. 1B).

As per claim 17, Zitlaw teaches the claimed invention as described above and furthermore, Zitlaw teaches that the SDRAM (i.e. 160 in Fig. 1B) is coupled to the controller (e.g. see Fig. 1B).

As per claims 18 and 19, Zitlaw teaches the claimed invention as described above and furthermore, Zitlaw teaches that the controller is adapted to selectively couple the DRAM memory array (using the chip select lines) to the synchronous memory interface; and selectively copy data from the non-volatile memory array and remap addresses of one or more DRAM memory array section to the synchronous memory interface to operate as "shadow" memory (e.g. see paragraph [0008]).

As per claims 20 and 21, Zitlaw teaches the claimed invention as described above and furthermore, Zitlaw teaches that the controller is adapted to operate the DRAM memory array (i.e. 160 in Fig. 1B) as (i) an extended read and/or write data buffer memory (i.e. 156 in Fig. 1B); and (ii) as "scratch pad" memory, i.e. the temporary or cache memory (e.g. see paragraph [0008] and Fig. 1B).

As per claims 22, 27, 45, 60, 75, 79, 94, 96 and 98-99, see arguments with respect to the rejection of claim 1. Claims 22, 27, 45, 60, 75, 79, 94, 96 and 98-99 are also rejected based on the same rationale as the rejection of claim 1.

As per claims 28, 46, 61, 80, 95 and 97, see arguments with respect to the rejection of claim 10. Claims 28, 46, 61, 80, 95 and 97 are also rejected based on the same rationale as the rejection of claim 10.

As per claims 34, 52, 67 and 86, see arguments with respect to the rejection of claim 11. Claims 34, 52, 67 and 86 are also rejected based on the same rationale as the rejection of claim 11.

As per claims 35, 44, 68 and 87, see arguments with respect to the rejection of claim 12. Claims 35, 44, 68 and 87 are also rejected based on the same rationale as the rejection of claim 12.

As per claim 54, see arguments with respect to the rejection of claim 13. Claim 54 is also rejected based on the same rationale as the rejection of claim 13.

As per claims 39-43, see arguments with respect to the rejection of claims 17-21. Claims 39-43 are also rejected based on the same rationale as the rejection of claims 17-21, respectively.

As per claims 55-59, see arguments with respect to the rejection of claims 17-21. Claims 55-59 are also rejected based on the same rationale as the rejection of claims 17-21, respectively.

As per claims 70-74, see arguments with respect to the rejection of claims 17-21. Claims 70-74 are also rejected based on the same rationale as the rejection of claims 17-21, respectively.

As per claims 89-93, see arguments with respect to the rejection of claims 17-21. Claims 89-93 are also rejected based on the same rationale as the rejection of claims 17-21, respectively.

7. Claims 1, 22, 27, 45, 60, 75, 79, 94, 96 and 98-99 are rejected under 35 U.S.C. 102(e) as being anticipated by McClain (USPN: 7,058,779).

As per claim 1, McClain teaches a non-volatile memory device comprising:

- a non-volatile memory array (i.e. 20 in Fig. 1);
- a buffer memory (i.e. 16 in Fig. 1);
- a synchronous memory interface (i.e. the SDRAM interface logic); and
- a controller (i.e. SDRAM memory controller in Fig. 2) coupled to the non-volatile memory array, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and buffer memory and to present the non-volatile memory device as a synchronous memory device through the synchronous memory interface (e.g. see Figs. 1-2 and the abstract).

As per claims 22, 27, 45, 60, 75, 79, 94, 96 and 98-99, see arguments with respect to the rejection of claim 1. Claims 22, 27, 45, 60, 75, 79, 94, 96 and 98-99 are also rejected based on the same rationale as the rejection of claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-4, 6-7, 23-26, 29-31, 47-49, 62, 65, 76, 78, 81 and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClain in view of McCormack et al. (USPN: 5,781,201) hereinafter, McCormack.

As per claims 2-3 and 6, McClain teaches the claimed invention as described above, but failed to teach the further limitation of buffering read and write data accesses to the non-volatile memory array in the buffer memory. McCormack, however, teaches about buffering both the read and write requests to the buffer memory (i.e. the video memory) allows the maximum bus utilization and minimizes the number of stalls in the system (e.g. see the Abstract). Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to modify the memory device of McClain as taught by McCormack so the overall performance of the memory device can be further improved.

As per claims 4 and 7, the combination McClain and McCormack teaches the claimed invention as described above, but both of them failed to teach about buffering read data accesses in a least recently used manner and write data accesses in a write-through manner. However, it is well known and notorious old in the art that by buffering read data accesses in a least recently used manner and write data accesses in a write-through manner reduces the data latency and improves the overall performance of the memory device. The common knowledge or well-known in the art statement is taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice made in the previous Office Action (see MPEP 2144.03 (C)).

As per claims 23, 29 and 47, see arguments with respect to the rejection of claim 2. Claims 23, 29 and 47 are also rejected based on the same rationale as the rejection of claim 2.

As per claims 24, 30, 48, 62, 76 and 81, see arguments with respect to the rejection of claim 3. Claims 24, 30, 48, 62, 76 and 81 are also rejected based on the same rationale as the rejection of claim 3.

As per claim 25, see arguments with respect to the rejection of claim 4. Claim 25 is also rejected based on the same rationale as the rejection of claim 4.

As per claims 26, 31, 49, 65, 78 and 84, see arguments with respect to the rejection of claim 6. Claims 26, 31, 49, 65, 78 and 84 are also rejected based on the same rationale as the rejection of claim 6.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClain in view of McCormack, further in view of Widdup (USPN: 6,651,148).

As per claim 5, the combination McClain and McCormack teaches the claimed invention as described above. However, none of them teaches that the controller is adapted to buffer a current data block to the non-volatile memory array in the buffer memory while accessing a sequentially following data block from the non-volatile memory array. Widdup, on the other hand, teaches about buffering both the read and write data (blocks) in the (buffer) memory to achieve the maximum bandwidth of the high-speed controller (e.g. see Col. 4, line 65 –Col. 5, line 1). Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current

invention was made to implement the teachings of Widdup in the memory device taught by the combination McClain and McCormack so the maximum bandwidth of the high-speed controller can be achieved.

10. Claims 8, 32, 50, 63-64, 77 and 82-83 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClain in view of McCormack, further in view of Wallace et al. (USPN: 6,628,537) hereinafter, Wallace.

As per claim 8, the combination McClain and McCormack teaches the claimed invention as described above. However, none of them teaches that the non-volatile memory device is adapted to indicate when the non-volatile memory device is busy by changing the status of one of an external "ready/busy" pin and a status register. Wallace, on the other hand, teaches that when the memory system is in process of executing a command and cannot receive another, a BUSY signal is written in the status register (i.e. 223 in Fig. 16) so the host computer wait until the current command/instruction is finish executing before sending the next one. Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to implement the teachings of Wallace in the memory device taught by the combination McClain and McCormack so the possible data corruption is avoided.

As per claims 32, 50, 63-64, 77 and 82-83, see arguments with respect to the rejection of claim 8. Claims 32, 50, 63-64, 77 and 82-83 are also rejected based on the same rationale as the rejection of claim 8.

11. Claims 9, 33, 51, 66 and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClain in view of Meyer (USPN: 4,065,862).

As per claim 9, the combination McClain, McCormack and Wallace teaches the claimed invention as described above. However, none of them teaches that the non-volatile memory device is adapted to indicate when the buffer memory device is full by asserting one of an external "ready/busy" pin and a status register. Meyer, on the other hand, teaches about asserting BUFFER FULL signal from the status register (i.e. 56 in Fig. 2), which would stop additional data to be sent to the buffer. Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to implement the teachings of Wallace in the memory device taught by the combination McClain, McCormack and Wallance so the possible data corruption is avoided by pausing the additional data transfer to the buffer memory while the buffer memory is full.

As per claims 33, 51, 66 and 85, see arguments with respect to the rejection of claim 9. Claims 33, 51, 66 and 85 are also rejected based on the same rationale as the rejection of claim 9.

12. Claims 14 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClain in view of Bartoli et al. (USPN: 6,442,068) hereinafter, Bartoli.

As per claim 14, McClain teaches the claimed invention as described above, but failed to teach that the non-volatile memory is adapted to have a burst data access mode. However, Bartoli teaches that the non-volatile memory is adapted to have a

burst data access mode (e.g. see Col. 2, lines 11-15). Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to utilize the burst data access mode in the non-volatile memory as taught Bartoli in the memory device taught by McClain. In doing so, (i) more data can be retrieved on each access; and (ii) it saves the bandwidth on the memory bus by sending less number of requests to the memory. Therefore, it is being advantageous.

As per claim 36, see arguments with respect to the rejection of claim 14. Claim 36 is also rejected based on the same rationale as the rejection of claim 14.

13. Claims 15-16, 37-38, 69 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClain in view of the 'Background of the Invention' section of the current application, hereinafter, BOI.

As per claims 15 and 16, McClain teaches the claimed invention as described above, but failed to teach that the controller is adapted to generate and evaluate ECC data. BOI, however, teaches that the controller of the flash memory generates the ECC code so the errors of the flash memory can be addressed by the OS/host/driver/firmware and/or the file system that the flash memory system formatted with (e.g. see paragraph [0005]). Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to generate and evaluate the ECC data by the controller as taught by BOI in the memory device taught by McClain for the benefit(s) stated above. The further limitation of generating the ECC

code in a hardware circuit is inherently present in the BOI because there has to be a hardware circuit present in order to generate the EC code.

As per claims 37, 69 and 88, see arguments with respect to the rejection of claim 15. Claims 37, 69 and 88 are also rejected based on the same rationale as the rejection of claim 15.

As per claim 38, see arguments with respect to the rejection of claim 16. Claim 38 is also rejected based on the same rationale as the rejection of claim 16.

Remarks

14. As to the remark, Applicant asserted that

(a) The system 150 of Zitlaw et al. is not disclosed as a memory device 156, 158, 160, but as a system 150. Applicant also maintains that Zitlaw et al. does not teach or disclose that the system 150 presents itself, and the coupled memory devices 156, 158, 160, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM.

(b) Applicant has carefully reviewed Zitlaw et al. and, in particular, Paragraph [0008] of Zitlaw et al., and can find no mention of the controller remapping addresses of one or more DRAM memory array sections to the synchronous memory interface to operate as "shadow" memory, or the utilization of the DRAM as an extended read and/or write data buffer memory, "scratch pad" memory, or temporary or cache memory. Applicant therefore respectfully maintains that Zitlaw et al. does not disclose using the DRAM memory

devices as a buffer memory "shadow" memory, scratch pad" memory, temporary or cache memory, or the controller being adapted to use the SDRAM as such.

(c) Examiner seems to interchangeably use memory array and memory device, and respectfully maintains that one skilled in the art would recognize them as not being interchangeable and that memory devices internally contain memory arrays and the control circuitry to support them.

(d) Applicant can find no mention of the controller remapping addresses of one or more DRAM memory array sections to the synchronous memory interface to operate as "shadow" memory, or the utilization of the DRAM as an extended read and/or write data buffer memory, "scratch pad" memory, or temporary or cache memory. Applicant therefore respectfully maintains that Zitlaw et al. does not disclose using the DRAM memory devices as a buffer memory "shadow" memory, scratch pad" memory, temporary or cache memory, or the controller being adapted to use the SDRAM as such.

(e) Applicant respectfully maintains that McClain discloses a personal computer system 10 having a system control logic ASIC 68 coupled to several memory devices 16, 18, 20, and not a memory device itself, as maintained by the Examiner.

(f) The rejection of claims 1-99 under 112, 2nd paragraph should be withdrawn as claims 1-99 clearly define and enable one of ordinary skills in the art to make and use the claimed invention.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), Examiner would like to point out to Applicant that the controller (i.e. 152 in Fig. 1B) of Zitlaw et al. prior art does present the non-volatile memory device (i.e. 150 in Fig. 1B) as a synchronous memory device (i.e. since each memory (156, 158 and 160 in Fig. 1B) of the non-volatile memory array can be synchronous memories, the memory device (150) as a whole functions a synchronous memory device) through the synchronous memory interface (i.e. 154 in Fig. 1B), as claimed in the current application (e.g. see Fig. 1B and paragraph [0036]).

With respect to (b), Examiner maintains that the Zitlaw et al. prior art clearly discloses that the decoder maps the individual memory device or portion of an individual memory device address range into the physical address range of the memory subsystem (e.g. see paragraph [0008]) and since the one or more memory devices (i.e. 156, 158, and 160 in Fig. 1B) are synchronous memory devices, it operates as shadow memory, i.e. by eliminating the need for separate shadow RAM in the system. Furthermore, the memory 156 in Fig. 1B of the Zitlaw et al. prior art is SDRAM memory and SDRAM memory is a 'fast' volatile memory, i.e. it can be used as read and/or write data buffer memory, "scratch pad" memory, or temporary or cache memory as claimed in this application (e.g. see paragraphs [0006] and [0008] and Fig. 1B).

With respect to (c), the Zitlaw et al. prior art teaches the memory device (i.e. 150 in Fig. 1B) having memory arrays (i.e. 158 and 160 in Fig. 1B) and a controller (i.e. 152 in Fig. 1B) as claimed and shown in Figs. 2, 3A and 3B of the current application.

With respect to (d), the Zitlaw et al. prior art does teach about remapping addresses of one or more DRAM memory array sections to the synchronous memory interface to operate as "shadow" memory by mapping the individual memory device or portion of an individual memory device address range into the physical address range of the memory subsystem. Chip select lines can also be used to map memory devices into the physical address range of the memory subsystem by selectively activating one or more individual memory devices for access as part of the address range of the memory subsystem in isolation from other addressable on the same memory interface bus (e.g. see paragraph [0008]).

With respect to (e), similar to the current claimed invention, McClain does teach a memory device (i.e. 10 in Fig. 1) having a non-volatile memory array (i.e. 20 in Fig. 1); a buffer memory (i.e. 16 in Fig. 1); a synchronous memory interface (i.e. the SDRAM interface logic); and a controller (i.e. SDRAM memory controller in Fig. 2). Examiner also would like to point out to Applicant that even though, similar to the McClain prior art, the component 204 in the Fig. 2 has a memory array (224), memory controller (212), the buffer memory (218), and the memory interface (232), it is called a memory device instead of a system.

With respect to (f), Examiner find no support in indicated paragraphs and/or drawings for the term "the external synchronous memory interface" used in claims 1-99. Therefore, 112, 2nd rejection of claims 1-99 is maintained. Examiner would like to suggest Applicant to particularly point out the specific paragraph/lines and/or drawing where the support the term indicated above can be found.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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